

TRANSMITTAL OF INFORMATION DISCLOSURE STATEMENT
(Under 37 CFR 1.97(b) or 1.97(c))

Docket No.
BUR920030045

In Re Application Of: Kiran V. Chatty

SEP 08 2003

Serial No.
10/604,922

Filing Date
August 27, 2003

Examiner
Unknown

Group Art Unit
Unknown

Title:

PFET-BASED ESD PROTECTION STRATEGY FOR IMPROVED EXTERNAL LATCH-UP ROBUSTNESS

Address to:

Assistant Commissioner for Patents
Washington, D.C. 20231

37 CFR 1.97(b)

1. The Information Disclosure Statement submitted herewith is being filed within three months of the filing of a national application other than a continued prosecution application under 37 CFR 1.53(d); within three months of the date of entry of the national stage as set forth in 37 CFR 1.491 in an international application; before the mailing of a first Office Action on the merits, or before the mailing of a first Office Action after the filing of a request for continued examination under 37 CFR 1.114.

37 CFR 1.97(c)

2. The Information Disclosure Statement submitted herewith is being filed after the period specified in 37 CFR 1.97(b), provided that the Information Disclosure Statement is filed before the mailing date of a Final Action under 37 CFR 1.113, a Notice of Allowance under 37 CFR 1.311, or an Action that otherwise closes prosecution in the application, and is accompanied by one of:

the statement specified in 37 CFR 1.97(e);

OR

the fee set forth in 37 CFR 1.17(p).

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PATENT & TRADEMARK OFFICE

PFET-BASED ESD PROTECTION STRATEGY FOR IMPROVED EXTERNAL LATCH-UP ROBUSTNESS

Payment of Fee

(Only complete if Applicant elects to pay the fee set forth in 37 CFR 1.17(p))

A check in the amount of _____ is attached.

The Assistant Commissioner is hereby authorized to charge and credit Deposit Account No. 09-0456 as described below. A duplicate copy of this sheet is enclosed.

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I certify that this document and fee is being deposited 09/05/03 with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20234, Box 1450, Alexandria, VA 22313

Signature

Signature of Person Mailing Correspondence

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Anthony J. Canale
Signature

Dated: 09/04/2003

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CC:



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:) Atty Docket No.: BUR920030045US1
)
 Kiran V. CHATTY et al.) Group Art Unit: To Be Assigned
)
 Serial No.: 10/604,922) Examiner: To Be Assigned
)
 Filed: August 27, 2003)
)
 For: PFET-BASED ESD PROTECTION)
 STRATEGY FOR IMPROVED)
 EXTERNAL LATCH-UP ROBUSTNESS)

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT
under 37 C.F.R. § 1.97(b)

Commissioner for Patents
Washington, DC 20231

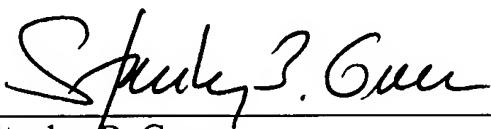
Sir:

Pursuant to 37 C.F.R. §§ 1.56 and 1.97, Applicants bring to the attention of the Examiner the documents listed on the attached PTO 1449. Copies of the listed U.S. Patent or U.S. Patent Application Publications are not provided in accordance with the waiver promulgated within the Notice published in 1276 OG 55, 05 August 2003. Copies of cited foreign patent documents and non-patent literature are submitted herewith in accordance with 37 CFR 1.98(a)(2). The filing of this Information Disclosure Statement shall not be construed as a representation that a search has been made, an admission that the information cited is, or is considered to be, material to patentability, or that no other material information exists.

Deposit Account Authorization

Authorization is hereby made to charge any fees due or outstanding, or credit any overpayment, to Deposit Account No. 09-0456 (International Business Machines Corporation).

Respectfully Submitted,



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Dated: August 27, 2003

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PTO/SB/08a/b (05-03)

Approved for use through 05/31/2003. OMB 0651-0031

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Substitute for form 1449/PTO				Complete if Known	
				Application Number	10/604,922
				Filing Date	August 27, 2003
				First Named Inventor	Kiran V. CHATTY
				Art Unit	To Be Assigned
				Examiner Name	To Be Assigned
Sheet	1	of	1	Attorney Docket Number	BUR920030045US1

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		2003/0062539	04-03-2003	Chatterjee	<i>already filed electronically on Sep 6, 2003.</i>
		4,669,177	06-02-1987	D'Arrigo et al.	
		5,543,650	08-06-1996	Au et al.	
		5,733,794	03-31-1998	Gilbert et al.	
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		6,228,726 B1	05-08-2001	Liaw	
		6,476,449 B1	11-05-2002	Lin	
		6,493,199 B1	12-10-2002	Su et al.	

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		✓ EP 1045444 A1	10-18-2000	Chen	<input checked="" type="checkbox"/> T ⁶
		✓ JP 10-50494	02-20-1998	Knight et al.	
		✓ JP 10-294445	11-04-1998	Szafranski et al.	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹ Applicant's unique citation designation number (optional). ² See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the application number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

NON PATENT LITERATURE DOCUMENTS					
Examiner Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			T ²
	/	Ming-Dou KER, "ESD Protection for CMOS Output Buffer by Using Modified LVTSCR Devices with High Trigger Current," IEEE Journal of Solid State Circuits, Vol. 32, No. 8, Aug. 1997, pp. 1293-96.			
	/	Ming-Dou KER and Hun-Hsien CHANG, "How to Safely Apply the LVTSCR for CMOS Whole-Chip ESD Protection without being Accidentally Triggered On," 1998 EOS/ESD Symposium, pp. 72-85.			
	/	Jeremy C. SMITH, "An Anti-Snapback Circuit Technique for Inhibiting Parasitic Bipolar Condition During EOS/ESD Events," 1999 EOS/ESD Symposium, pp. 62-69.			
	/	Teruo SUZUKI et al., "A Study of Fully Silicided 0.18um CMOS ESD Protection Devices," 1999 EOS/ESD Symposium, pp. 78-87.			
	/	Gianluca BOSELLI et al., "Efficient pnp Characteristics of pMOS Transistors in Sub-0.13um ESD Protection Circuits," 2002 EOS/ESD Symposium, pp. 257-66.			

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹Applicant's unique citation designation number (optional). ²Applicant is to place a check mark here if English language Translation is attached.

Examiner Signature		Date Considered	
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